The opinion in support of the decision being entered today was ***not*** written for publication and is ***not*** binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte RICHARD T. BEHRENS, LI DU, WILLIAM G. BLISS, DAVID E. REED and MARK S. SPURBECK

_____

Appeal No. 1999-1449
Application 08/640,351

_____

ON BRIEF

_____

Before HAIRSTON, FLEMING, and RUGGIERO, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 and 3-18, all the claims pending in the present application. Claims 2, 19 and 20 have been cancelled.

The invention relates generally to a sampled amplitude read channel for reading discrete time sample values (Xk) (25) generated by sampling an analog read signal (19) from a read head positioned over a magnetic read medium (18). See figure 3, and

specification, page 1, lines 14-18. The sampled amplitude read channel includes a sampling device (24) that asynchronously samples the analog read signal to generate discrete time sample values (Xk) (25). See figure 3, and specification, page 14, lines 4-5. The sampled amplitude read channel further includes an adaptive equalizer (B103), responsive to the discrete time sample values (Xk) (25) for generating equalized sample values (32) according to a target response. See specification, page 14, lines 4-9. The sampled amplitude read channel also includes an interpolated timing recovery circuit (B100) for generating interpolated sample values (B102). See figure 3 and specification, page 20, lines 1-3. Additionally, the sampled amplitude read channel includes a discrete time sequence detector (34) for detecting the digital data from the interpolated sample values (B102).

Figure 4B is a detailed block diagram of the interpolated timing recovery circuit (B100) shown in figure 3. See Specification, page 11, lines 11-13, and page 19, lines 14-15. Figure 8B is a detailed block diagram of the adaptive equalizer (B103) shown in figure 3. See Specification, page 11, lines 22-23, and page 35, lines 17-18. Figure 8C is an alternative embodiment of the detailed block diagram of the adaptive

equalizer (B103) shown in figure 3. See Specification, page 11, lines 24-25, and page 36, lines 19-24.

The adaptive equalizer (B103) comprises an FIR filter (C100) having a plurality of filter coefficients (C116). See figures 8B, 8C, and specification, page 35, lines 19-21, page 37, line 2. The adaptive equalizer (B103) is further responsive to an error value, e_k, (C112) computed as a function of the output (Y_{k+t}) (B102) of the FIR filter (C100) and an estimated ideal value ($\sim Y_{k+t}$). See figures 8B, 8C specification, page 36, lines 4-10. Additionally, the adaptive equalizer (C100) comprises an interpolation circuit (C106), responsive to the interpolated sample values (Y_{k+t}) (B102) for generating the error value, e_k, (C112) synchronous with the discrete time sample values (X_k) (25). See figures 8B, 8C, and specification, page 36, lines 10-18.

The only independent claims 1 and 17 present in the application are reproduced as follows:

1. A sampled amplitude read channel for reading digital data from a sequence of discrete time sample values generated by sampling an analog read signal from a read head positioned over a magnetic medium, comprising:

(a) a sampling device for sampling the analog read signal to generate the discrete time sample values;

(b) an adaptive equalizer, responsive to the discrete time sample values, for generating equalized sample values according to a target response;

(c) an interpolated timing recovery circuit for generating interpolated sample values; and

(d) a discrete time sequence detector for detecting the digital data from the interpolated sample values,

wherein:

the adaptive equalizer comprises an FIR filter comprising a plurality of filter coefficients;

the adaptive equalizer is responsive to an error value e_k computed as a function of an output of the FIR filter and an estimated ideal value;

the adaptive equalizer comprises an interpolation circuit, responsive to the interpolated sample values, for generating the error value e_k synchronous with the discrete time sample values.

17. A method for reading digital data from a sequence of discrete time sample values generated by sampling an analog read signal from a read head positioned over a magnetic medium, wherein the analog read signal comprises pulses modulated by the digital data at a predetermined baud rate, the method comprising the steps of:

(a) asynchronously sampling the analog read signal to generate asynchronous sample values;

(b) adaptively equalizing the asynchronous sample values to generate equalized sample values according to a target response, comprising the steps of:

(i) computing an error value as a function of a baud rate synchronous sample value and an estimated ideal sample value; and

(ii) synchronizing the error value to the asynchronous sample values; and

(c) interpolating the equalized sample values to generate the baud rate synchronous sample values; and

(d) detecting the digital data from the baud rate synchronous sample values.

The Examiner relies on the following references:

Minuhin	5,650,954	Jul. 22, 1997 (filed Jan 30, 1996)
Spurbeck et al. (Spurbeck)	5,696,639	Dec. 9, 1997 (filed May 12, 1995)
Nowak et al. (Nowak)	5,561,598	Oct. 1, 1996 (filed Nov. 16, 1994)

Claims 1 and 3 through 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Spurbeck and Minuhin and Nowak.

Claims 17 and 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Spurbeck and Minuhin.

Rather than reiterate the arguments of Appellants and the Examiner, the opinion refers to respective details of the Brief and Examiner's Answer.

OPINION

After a careful review of the evidence before us, we do not agree with the Examiner that claims 1 and 3-16 are properly rejected under 35 U.S.C. § 103 as being unpatentable over Spurbeck and Minuhin and Nowak, nor do we agree with the Examiner that claims 17 through 18 are properly rejected under 35 U.S.C.

§ 103 as being unpatentable over Spurbeck and Minuhin. Thus, we will reverse the rejection of claims 1 and 3-18.

We turn first to the rejection of claims 1 and 3-16 under 35 U.S.C. § 103 as being unpatentable over Spurbeck in view of Minuhin and Nowak.

The Examiner bears the initial burden of establishing a ***prima facie*** case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed. Cir. 1992). ***See also In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ at 1444. ***See also Piaseki***, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must

necessarily weigh all of the evidence and arguments." ***In re Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***, Slip OP 00-1158, page 9. With these principles in mind, we commence the review of the pertinent evidence and arguments of Appellants and Examiner.

Appellants argue on pages 8 and 9 of the Brief that although Nowak discloses an adaptive equalizer, Nowak does not teach or suggest an interpolation circuit for generating error values synchronous to the channel rate. Appellants argue that Nowak's figures 3-4 do not disclose Appellants' claimed interpolation circuit because the discrete time values are already synchronized to the error values. Consequently, they do not need to be interpolated to generate error values synchronous with the channel rate.

In particular, on pages 9 and 10 of the Brief, Appellants state the following:

> The reason that Nowak does not disclose an interpolation circuit is because the discrete time sample values X(k) (48) in figs. 2, 3 and 4, are already

> synchronized to the error values e(k) (52). There is no reason to interpolate to generate the error values synchronous to the channel rate.
>
> In the present invention, the read signal **62** of FIG. 3 is sampled asynchronous to the baud rate. The asynchronous samples **32** are processed by an interpolated timing recovery circuit **B100** to generate interpolated sample values **B102** that are synchronous to the baud rate. As shown in FIG. 8B, the synchronous sample values **B102** are used to generate an error value e_{k+t} **C104** that is also synchronous to the baud rate. However, the coefficient update circuit **C114** requires the error values e_k to be synchronous to the channel samples X_k 25 rather than synchronous to the baud rate. Therefore, as shown in FIG. 8B, the present invention provides an interpolation circuit **C106** for interpolating the baud rate synchronous error values e_{k+t} **C104** to generate error values e_k **C112** synchronous to the channel samples X_k **25**. Again, Nowak does not discloses or suggest this aspect of the invention because in Nowak, the input sample values X(k) (48) are synchronous to the baud rate and thus already synchronous to the error values e(k) (52). Therefore, there is no need to interpolate the error values e(k) (52) in order to synchronous the error values e(k) to the channel samples X(k) (48) as in the present invention. The same argument applies to the alternative embodiment of the present invention shown in FIG. 8C.

In order for us to decide the question of obviousness, "[t]he first inquiry must be into exactly what the claims define." **In re Wilder**, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "Analysis begins with a key legal question-- what is the invention claimed ?" . . . Claim interpretation . . . will normally control the remainder of the decisional process."

Panduit Corp. v. Dennison Mfg., 810 F.2d 1561, 1567-68, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), **Cert denied**, 481 U.S. 1052 (1987).

We note that claim 1 reads as follows:

> the adaptive equalizer comprises an interpolation circuit, responsive to the interpolated sample values, for generating the error value e_k synchronous with the discrete time sample values.

On page 35, line 17 through page 36, line 18, Appellants' specification discloses that the sample values, X(k), are provided to the adaptive equalizer B103 shown in figure 8B of the sample rate of the A/D (24). Figure 8B shows that the adaptive equalizer B103 includes an FIR filter C100 and an interpolator circuit B122. In particular, Appellants' specification states that:

> Because the FIR filter **C100** operates on the sample values prior to the interpolated timing recovery loop **B100**, its order can be increased over the prior art without adversely affecting the latency of timing recovery (i.e., the number of filter coefficients can be increased).
>
> The output Y_k **32** of the FIR filter **C100** is input into the interpolator **B122** for generating the interpolated sample values Y_{k+t} **B102**. The interpolated sample values Y_{k+t} **B102** are input into a slicer **B141** (FIG 4B) which generates estimated sample values $\sim Y_{k+t}$. The estimated sample values $\sim Y_{k+t}$ are subtracted from the interpolated sample values Y_{k+t} at adder **C102** to generate a sample error value e_{k+t} **C104** that is synchronized to the baud rate rather than the sample rate. Because the LMS algorithm operates on sample values X_k at the sample rate, it is necessary to convert the error value e_{k+t} **C104** into an error value e_k **C112** synchronous to

> the sample rate. This is accomplished by an interpolation circuit **C106** which computes an interpolated error value e_k **C112** from the baud rate error values e_{k+t} **C104.** Preferably, the error value interpolation circuit **C106** is implemented as a first order linear interpolation, but it may be a simple zero order hold, or a more complex interpolation filter as described above.

Thus, the claim does require that the interpolation circuit (C106) synchronize the error values e(k) to the channel sample values X(k) (25), the claimed discrete-time sample values.

We agree with Appellants that Nowak does not teach or suggest an interpolation circuit, which interpolates the error value e(k) in order to synchronize the error values e(k) to the channel sample values Xk, as claimed. We note that Nowak's input sample values are already synchronous to the error values. Nowak discloses an adaptive control system 39, which includes an adaptive control filter 46 for outputting a correction signal Yk in response to an input signal Xk. The adaptive control filter further includes an error sensor 54 for generating an error signal e(k) to adapt the adaptive control filter. See Nowak, column 3, lines 18 through 35. Thus, Nowak is not concerned with the problem that Appellants' invention seeks to resolve. Specifically, Nowak does not seek to compensate for parameter variations while reading data across the radii of a magnetic disk. Hence, Nowak does not have a need to synchronize the input

values Xk to the baud rate, and subsequently to the channel rate, as in Appellants' invention. Therefore, we will not sustain the Examiner's rejection of claims 1 and 3-16.

We now, turn to the rejection of claims 17-18 under 35 U.S.C. § 103(a) as being unpatentable over Spurbeck and Minuhin. Appellants argue on pages 8 and 9 of the Brief that the references do not teach or suggest generating error values synchronous to the channel rate.

Claim 17 recites a method for reading digital data from a sequence of discrete time sample values (Xk) (25) generated by sampling an analog signal (19) read from a read head positioned over a magnetic medium (18). See figure 3, and specification, page 1, lines 14-18. The claimed method comprises the step of asynchronously sampling the analog read signal (19) to generate asynchronous sample values (25). See figure 3, and specification, page 14, lines 4-5. The claimed method further comprises the step of adaptively equalizing the asynchronous values (25) to generate equalized sample values (32) (Y(n)) according to a target response. See figure 3, and specification, page 14, lines 4-9. The step of adaptively equalizing the asynchronous values further comprises the step of computing an error value, e_k, (C112) as a function of a baud rate synchronous

sample value (Y_{k+t}) and an estimated ideal sample value ($\sim Y_{k+t}$), and the step of synchronizing the error value, e_k, to the asynchronous sample values (Xk) (25). See figures 8B, 8C, specification, page 36, lines 4-10. Additionally, the claimed method comprises the step of interpolating the equalized sample values (32) to generate baud rate synchronous sample values (B102). See figures 8B, 8C, and specification, page 36, lines 10-18. Last, the method comprises the step of detecting digital data from the baud rate synchronous to the sample values (Xk) (25). See figure 3, and specification, page 17, lines 24 through page 18, line 1. Thus, Appellants' claim 17 requires method steps performed by the interpolation circuit (C106) to synchronize the error values e(k) to the channel sample values X(k) (25), the claimed asynchronous sample values. Therefore, we will not sustain the Examiner's rejection of claims 17 and 18 for the same reasons discussed above.

Accordingly, the decision of the Examiner rejecting claims 1 and 3 through 18 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
	)	BOARD OF PATENT
MICHAEL R. FLEMING	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
JOSEPH F. RUGGIERO	)	
Administrative Patent Judge	)	

MRF:pgg

Cirrus Logic Inc.
Intellectual Property Department
3100 West Warren Avenue
Fremont, CA 94538-6423